

REMARKS

Claims 1-29 are pending in the instant application. Claims 1-25 presently stand rejected. Claims 1, 2, 3, 5, 8, 10, 14, 21, and 24 have been amended. Claims 11, 12, 19, 23 have been canceled. No new matter has been added. Entry of this amendment and reconsideration of the pending claims are respectfully requested.

Claim Rejections – 35 U.S.C. § 103

Claims 1, 4-9, 12-14, 17-22, and 25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Banerjee (US 6,820,127 B2) in view of Brustoloni (US 6,625,149 B1). Claims 2, 3, 10, 11, 15, 16, 23, and 24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Banerjee (US 6,820,127 B2) in view of Brustoloni (US 6,625,149 B1) as applied to claims 1, 8, 14, and 21, and further in view of Ganfield (US Pub. No. 20040218631).

Claim 1 as amended recites:

A method comprising: receiving a packet at a network device; pre-fetching a protocol control block (PCB) associated with the packet into a cache of a selected processing unit; queuing the packet for processing; pre-fetching a header associated with the packet into the cache of the selected processing unit; and retrieving the PCB from the cache of the selected processing unit when the selected processing unit is ready to process the packet.

In contrast, the combined references do not teach or suggest (at least) the above-emphasized portion of the claim. The office action (item 10) concedes that the combined references of Banerjee and Brustoloni fails to disclose a method, apparatus and further comprising pre-fetching a header associated with the packet in cache.

However, Ganfield fails to overcome the deficiency of Banerjee and Brustoloni because the buffer descriptor cache of Ganfield is not a cache of the selected process unit. Instead the buffer descriptor cache 530 is coupled to the control processor 104 and the data flow processor 106 (paragraph 22, Fig. 1). The buffer descriptor cache of Ganfield is not a cache of the selected process unit because the buffer descriptor cache is coupled between the control processor and the data flow processor.

The Office Action asserts that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combination of Banerjee and Brustoloni because it would minimize processor time by minimizing latency. The applicants traverse this assertion as being general, not directed to claim distinctions, and not directed to the claim as a whole. Applying the reasoning broadly, any invention that minimizes processor time by minimizing latency would be reasoned to be prima-facie obvious.

Claims 8, 14, and 21 are allowable at least for the reasons stated for claim 1. Dependent claims are at least allowable for the reasons from which they depend are allowable.

CONCLUSION

In view of the foregoing amendments and remarks, it is believed that the applicable rejections have been overcome and all claims remaining in the application are presently in condition for allowance. Accordingly, favorable consideration and a Notice of Allowance are earnestly solicited. The Examiner is invited to telephone the undersigned representative at (206) 292-8600 if the Examiner believes that an interview might be useful for any reason.

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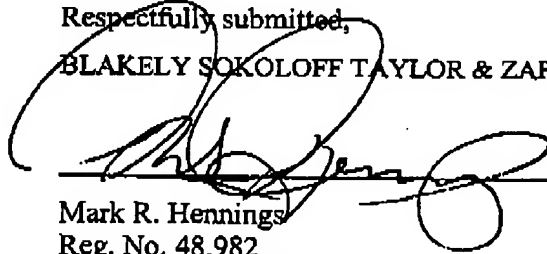
It is not believed that extensions of time are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a). Any fees required therefore are hereby authorized to be charged to Deposit Account No. 02-2666. Please credit any overpayment to the same deposit account.

Respectfully submitted,

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP

Date:

10/1/07


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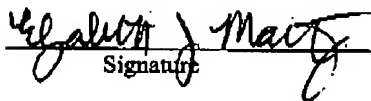
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